Even if it is assumed that the CPU 12 has an integral ROM memory, this does not teach a packaged device that includes a volatile memory since a ROM is not a volatile memory and it certainly does not teach a packaged device that includes a cross point memory.

With respect to the argument that hundreds of chips may be packaged together, even if this is so, and even if it is intended to refer to dice by the word chips, it still does not teach packaging the particular claimed elements together as claimed.

Therefore, reconsideration of the rejection of claim 1 is respectfully requested.

The office action indicates that no information is provided in claim 1 about the configuration of the various elements. But dependent claims, that were not allowed, point these elements out. For example, claim 5 calls for the use of stacked dice. Claim 6 calls for a folded stack package. Claim 9 calls for a ball grid array package.

Claim 11, dependent on claim 10, calls for packaging a volatile memory on a separate die in a package. Claim 12 calls for a folded stacked package. Claim 15 calls for stacking the dice one on top of the other. Claim 17 also calls for a ball grid array package.

Claim 18 calls for a packaged integrated circuit in which the processor and the cross point memory are on separate dice within the integrated circuit package. Certainly this is no where suggested in any of the cited references. Claim 19 calls for a third die with a volatile memory. There is no suggestion of putting each of those three elements on separate dice. Claim 22 calls for stacked dice, claim 23 calls for a folded stack package, and claim 24 calls for a ball grid array package.

In view of these remarks, reconsideration of the rejection is respectfully requested.

Respectfully submitted,

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